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Evaluation of Inverter Reliability Performance Due to Negative Bias Temperature Instability (NBTI) Effects in Advance CMOS Technology Nodes

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ABSTRACT

Negative bias temperature instability (NBTI) is the most concern issue CMOS devices with the scaling down of the CMOS technologies. NBTI effect contributes to P-MOSFET device degradation which later reduce the performance and reliability of CMOS circuits. This paper presents a reliability simulation study based on R-D model on CMOS inverter circuit. HSPICE MOSRA model together with the Predictive Technology Model (PTM) was used as to incorporate the NBTI model in the circuit reliability simulation study for different technology nodes. PTM of High Performance (HP) models of 16nm, 22nm, 32nm and 45nm were used in this simulation study. The atomic hydrogen based model was integrated in the simulation. The results show that in a CMOS inverter circuit, the threshold voltage shift of p-MOSFET under NBTI stressing increased as the year progressed.. The threshold voltage shift was observed to increase up to 45.1% after 10 years of operation. The time exponent, n ~ 0.232 of the threshold voltage shift observed indicates that the defect mechanism contributed to the degradation is atomic hydrogen. The propagation delay increased to 19.5% over a 10-year period. s up to 19.5% from the zero year of operation until 10 years of the operation. In addition, the time propagation delay increased as year increased when the technology nodes smaller. The finding is important for understanding reliability issues related to advanced technology nodes in CMOS circuits study.

Keywords: NBTI, CMOS Inverter, Predictive Technology Model, HSPICE MOSRA, circuit reliability

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INTRODUCTION

Negative bias temperature instability (NBTI) is a well-known issue in CMOS devices compared to other issues such as hot carrier injection (HCI). Since it is first reported in the 1960s (Deal et al., 1967) many researchers

are studying the NBTI properties to see its impact on CMOS devices and a several ways to reduce the degradation effect.

NBTI increases with an increase of negative stress gate bias (V_G), temperature (Ho et al., 2013) and NBTI shows power-law time dependence for moderate to very long stress time (t-stress) (Haggag et al., 2007) which can be described with an empirical description below :

$$\Delta V_{TH} \approx C \exp\left(-\frac{E_A}{k_B T}\right)\left(\frac{|V_G - V_{TH0}|}{t_{OX}}\right) t_{stress}^{n} \quad (1)$$

where E_A is an apparent activation energy (typically in range of 60-80 meV), k_B is the Boltzmann constant, T is a temperature, V_G is a negative stress gate bias, t_{OX} is an oxide thickness, and n is a power-law time exponent with range between 0.1 and 0.25 (Franco et al., 2014). An oxide electric field ($E_{ox} \approx |V_G - V_{TH0}| / t_{ox}$) clearly shown to be another parameter which lead to NBTI degradation by varying t_{ox}. Hence, an idea of implementing that features to study on the circuit reliability and performance were used in this work.

According to Mahapatra (Mahapatra et al., 2013), the author declared that NBTI results in positive charge build-up in the gate insulator and causes temporal shift in device parameters such as linear and saturation drain currents (ΔI_{DLIN} and ΔI_{DSAT}), subthreshold slope (ΔS), threshold voltage (ΔV_{TH}), and transconductance (Δ_{gm}). Threshold voltage shift (ΔV_{TH}) due to NBTI effect gives a fractional change of drain current for MOSFETs in both linear (2) and saturation region (3). MOSFETs in the saturation region shown twice degradation than in the linear region.

$$I_{Dlin} \approx \frac{W \mu_{eff} C_{OX}}{L}(V_G - V_T)V_D \Rightarrow \frac{1}{I_D}\frac{dI_D}{dV_T} = -\frac{\Delta V_T}{V_G - V_T} \quad (2)$$

$$I_{Dsat} \approx \frac{W \mu_{eff} C_{OX}}{L}(V_G - V_T)^2 \Rightarrow \frac{1}{I_D}\frac{dI_D}{dV_T} = -\frac{2\Delta V_T}{V_G - V_T} \quad (3)$$

The delay time is:

$$t_d = \frac{C|V_{DD}|}{I_D} = \frac{2LC}{W \mu_{eff} C_{ox}(V_{DD} - V_T)^2} \quad (4)$$

where C is the capacitance and V_{DD} the supply voltage. Since NBTI effect results in reducing of μeff and increasing of V_T, the delay time is also increase (Schroder, 2007).

Inverters, the nucleus of all digital designs which simplified the designing process for complex structures such as NAND gates, flip-flop and microcontroller once its operation and properties are clearly understood (Berkeley, 1999). NBTI effect on the inverter can be studied to see its impact on the inverter reliability performance.

Finding on aging analysis and design (Parthasarathy et al., 2014) which focused NBTI study on propagation delay shown that threshold voltage change causes an increase in the propagation delay. NBTI studies on power gating designs (Lee et al., 2011; Rossi et al., 2016) shown that NBTI does not affect the average power. However, the result of power gating design is used to study the device performance based on the device lifetime. Technology scaling causes the nominal voltage decreases which results in slower switching speeds (Bild et al., 2011).

In this paper, the effect of inverter performance and reliability on NBTI degradation are investigated based on increasing the threshold voltage. Propagation delay, switching speed, noise margin and average power consumption of different parameter stress are analyzed and discussed in section III.

METHODOLOGY

The inverter circuit was used to perform a reliability and performance study using the built-in aging models integrated into Synopsys HSPICE. MOSFET Model Reliability Analysis (MOSRA) was used to predict the long-term reliability and performance of the device. The reliability and performance of a CMOS technology become more challenging as the technology is scaled down. NBTI degradation shown to increase with an increase of negative stress gate bias (VG) in the previous study(Ho et al., 2013). However, oxide field (EOX) also plays an important role on the NBTI degradation effect (Chenouf, Djezzar, Benadelmoumene, Tahi, & Goudjil, 2015).

A high performance (HP) of PTM technology models were used with different technology nodes (16nm to 45nm). A nominal supply voltage(Vdd) based on each technology parameter was used for the different technology sizes. The simulation was simulated under a 10 years of stress time and constant temperature of 27oC. The inverter sizing ratio for NMOS used in this simulation was 2:1. The width and length (W/L) for PMOS is twice than NMOS which was 4:1. For example, W/L for PMOS and NMOS used for HP 16nm technology were 64nm/16nm and 32nm/16nm respectively.

Then, the NBTI model will be implemented in MOSRA flow for HSPICE circuit simulation as shown in Figure 1. EOL (end of lifetime) of a MOSFET device can be described as the device operation time where a key measure of device performance, such as I_{dsat}, degrades by a given percentage (typically, 10%) of its fresh (un-aged) value (Synopsys, 2009). The inverter was simulated under a two-phase simulation (pre-stress simulation phase and post-stress simulation phase) in the MOSRA flow.

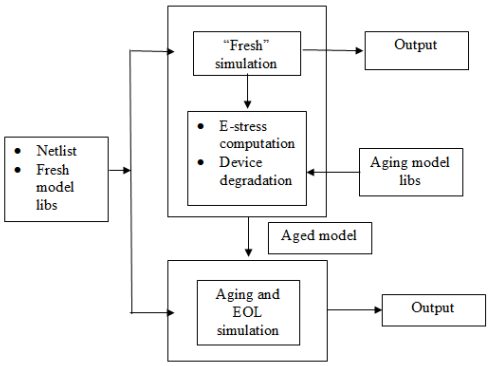

Figure 1. HSPICE MOSRA process flow

The result is then extrapolated to calculate the total device performance degradation after a user-specified time of circuit operation (age) (Synopsys, 2009). Threshold voltage shift (ΔV_{TH}) was calculated The rise time, fall time and average power consumption can be obtained by referring to HSPICE design hierarchy (Nekovei, 2006). The rise time and fall time were used to calculate the propagation delay. Transient analysis was used to obtain the rise/fall time and average power consumption while DC analysis was used to obtain switching speed (Akshay Sridharan, 1988a, 1988b). The Voltage Transfer Curve (VTC) can be plotted by using Synopsys CosmosScope after the DC analysis simulation. Later, noise margin can be obtained from the VTC.

RESULT AND DISCUSSION

In this section, the effect of NBTI on threshold voltage shift (ΔV_{th}) of p-MOSFETs and the circuit performance in terms of propagation delay (t_{pd}), switching speed, and average power dissipation of an inverter were analysed based on year of operation and different technology nodes.

Aging Effect

Years of operation are from1 year to 10 years and measured at year 1, year 5 and year 10. The behavior of the inverter in terms of the threshold voltage shift, propagation delay, switching speed and average power dissipation was observed and analyzed. The factors that cause the change in the inverter behavior were identified according to device year of operation and different technology nodes.

Figure 2 shows that as the years of operation increases, the threshold voltage shift, ΔV_{th} also increases. The inverter with 1 year of operation produced less ΔV_{th} than 5 years and 10 years. As a result, ΔVth increases up to 45.1% from the first year to 10 years of operation. ΔV_{th} follows a power-law of the stress time using formula in (1). Based on the graph, A is equal to 0.0559 with n equal to 0.232. Thus, from the result the graph follows the power-law of the stress time where n ~ 0.25 reflects that the atomic hydrogen is the defect mechanism (Franco et al., 2014).

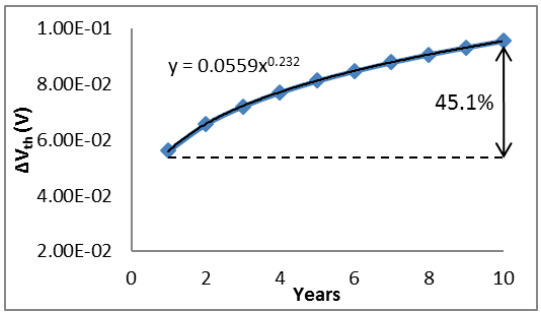

Figure 2. The relationship between threshold voltage shift and aging year

Next, Figure 3 shows that as the inverter aged year increases, the propagation delay, t_{pd} also increases. The lowest propagation delay between the measured years of operation is during the zero year of operation. The propagation delay increase over 10 years and increases up to 19.5% from the zero year of operation until 10 years of the operation. As a conclusion, the propagation delay increases as the stress time increases. This is similar to previous work where the propagation delay increased due to NBTI effects (Parthasarathy et al., 2014).

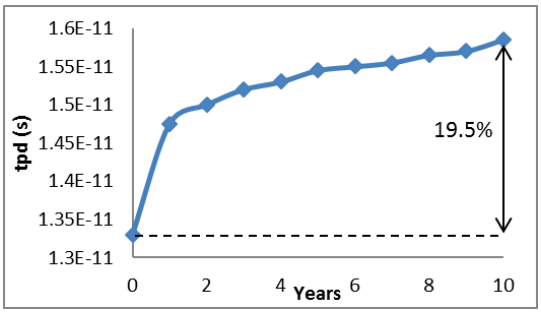

Figure 3. The relationship between propagation delay and aging year

However, the switching speed for the inverter remains constant in Figure 4 for each 1 year, 5 years and 10 years. This is due to constant ratio of W/L is used during the simulation. V_M can be increase by larger ratio which mean making the PMOS wider (Parthasarathy et al., 2014). Since the W/L ratio used remains the same, so there is no change in switching speed. It can be concluded that the switching speed does not affected by NBTI.

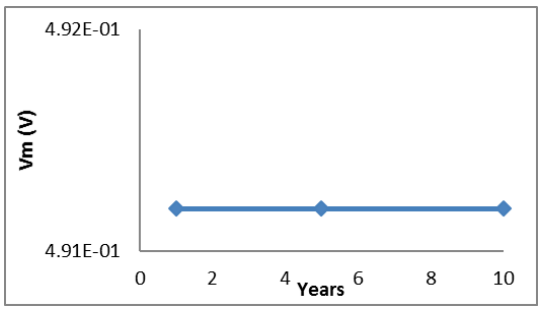

Figure 4. The relationship between switching speed and aging year

Another limiting factor in designing nano-scale circuits is the power dissipation. Hence, in this work, we include the analysis NBTI effect on power dissipation. As shown in Figure 5, the average power dissipation of the inverter is shown to be not affected by the NBTI as it is decreases as the year increases (Rossi et al., 2016). This is in agreement with (Wang & Zwolinski, 2008) where the delay that increase due to NBTI does not cause an increase in the power dissipation. The average power dissipation of 10 years of operation is lower than 1 year

of operation and at the same value during the 5 years of operation. It decreases by 4% from the start of operation until 10 years of operation. A capacitive coupling between input and output will trigger an injection of current into the supply, when the output briefly overshoots V_{DD} (Berkeley, 1999). As a result, it decreases exponentially inconsistent over 10 years and generate lesser power dissipation from zero year to 10 years of operation.

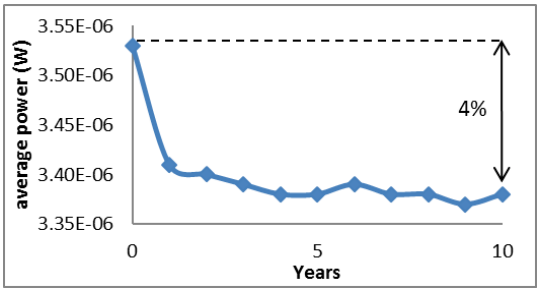

Figure 5. The relationship between average power and aging year

Technology scaling

Scaling down technology node is a design technique that is used to improve the inverter performance. The technology nodes were varied from 16nm to 45nm and measured. Each PTM model uses different voltage supply such 0.7V, 0.8V, 0.9V, and 1.0V for 16nm, 22nm, 32nm and 45nm respectively. A comparison between models was done to study its effect on inverter performance.

As shown in Figure 6, ΔV_{th} decreases as the technology nodes decreases. Over 10 years of operation, HP 16nm model produces the least ΔV_{th} than other HP models. ΔV_{th} of HP 16nm model are reduces up to 26.5%, 18.1% and 9.7% respectively from HP 45nm, HP 32nm and HP 22nm at 10 years of operation. Therefore, threshold voltage shift decreases as the technology models become smaller.

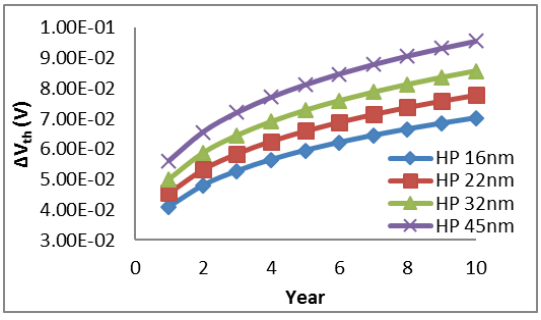

Figure 6. The relationship between threshold voltage shift and device lifetime for different technology scaling over 10 years

Figure 7 depicts the propagation delay trend for different technology nodes over device lifetime. The propagation delay increases as the technology node decreases. HP 45nm model shows the best propagation delay compared to other HP models. The propagation delay of HP 16nm model increases by 31.5%, 22% and 10% for HP 45nm, HP 32nm, and HP 22nm respectively. As the technology nodes become smaller, the nominal voltage supply, V_{DD} become smaller. Since the W/L ratio is constant, smaller V_{DD} is commonly used by designer to improve average power consumption as a trade-off to the propagation delay (Berkeley, 1999). Thus, the worst-case scenario for the propagation delay for the PTM model is HP 16nm model with the lowest voltage supply of 0.7V which evidence that the smaller technology will lead to poor reliability performance of CMOS inverter circuit.

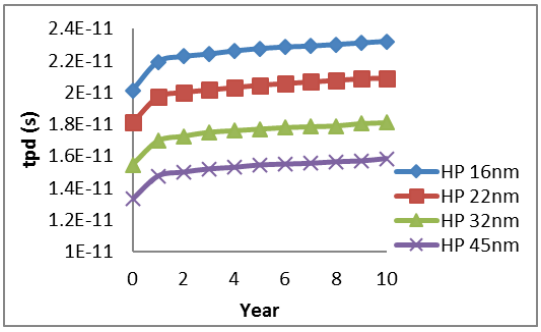

Figure 7. The relationship between propagation delay and device lifetime for different technology scaling over 10 years

Although switching speed and average power does not effected by NBTI, the inverter performance was evaluated. The switching speed (V_{sp}) of the inverter decreases as the technology node decreases by referring to Figure 8. HP 16nm model show the lowest V_{sp} compared with other model. V_{sp} was reduced by 26.1% from HP 45nm model to HP 16nm model. Switching speed reduces as the nominal supply voltage decreases from the technology scaling. Reducing nominal supply voltage will results in lower oxide field, Eox which was in agreement with (Chenouf, Djezzar, Benadelmoumene, Tahi, & Goudjil, 2015).

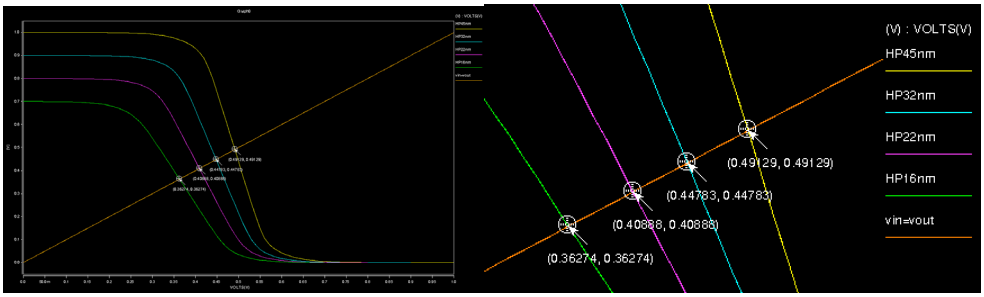

Figure 8. Switching speed and technology scaling

Based on the VTC graph above, noise margin for high logic level (NMH) and low logic level(NML) were obtained. Noise margins were evaluated to see how well the gate perform under noisy condition. Basically, an ideal noise margin is when $NM_H = NM_L = VDD/2$. Table 1 shows the noise margins that were obtained from VTC graph. The noise margin decreases as the technology model becomes smaller. Smaller technology nodes results in decreasing of the threshold voltages. Decreasing the threshold voltage leads to reducing the threshold voltage shift. It was observed that noise margin decreases as the threshold voltage decreases in the previous study (Mukherjee, Mondal, & Reddy, 2010). Thus, it can be concluded that somehow threshold voltage has a relationship with noise margin.

Table 1
Noise margin for different technology models

Technology Models	V_{OH} (V)	V_{IH} (V)	N_{MH} (V)	V_{OL} (V)	V_{IL} (V)	N_{ML} (V)
HP 16nm	0.7	0.475	0.225	0	0.25	0.25
HP 22nm	0.8	0.525	0.275	0	0.30	0.30
HP 32nm	0.9	0.55	0.35	0	0.35	0.35
HP 45nm	1.0	0.575	0.425	0	0.40	0.40

Average power consumption reduction is mainly because of using a low supply voltage. Figure 9 shows that HP 16nm model has lower average power consumption compared to other models. In HP 16nm models average power reduction is 59.4% than of HP 45nm models at 10 years of device lifetime. Since NBTI mainly focused on threshold voltage shift and not voltage supply. It can be concluded that NBTI effect does not influence the average power consumption compared with the NBTI aging effect (Rossi et al., 2016). Hence, average power consumption reduce as the supply voltage decreases due to technology and the device stress time increases.

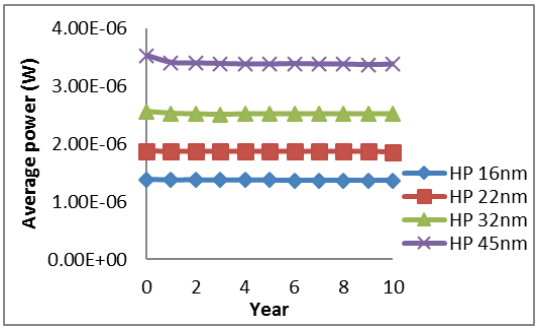

Figure 9. The relationship between average power and device lifetime for different technology scaling over 10 years

CONCLUSION

In this paper, the study of inverter performance and reliability following increases voltage which leads to NBTI degradation was undertaken. Aging effect and technology scaling are the parameters used to study the NBTI effect on device performance and reliability. Results

threshold voltage shift increases as the stress time increases and the technology model increases. In addition, the propagation delay increases as the stress time increases and technology model decreases. Stress time gives no effect on the switching speed, but smaller technology model gives smaller switching speed. Noise shown to decrease as the technology model decrease. The average power consumption is not affected by NBTI which it is reduced as the stress time increases and the technology model becomes smaller.

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